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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,629	03/18/2004	Wei Kuo	AUS920040030US1	5818

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EXAMINER	
UNELUS, ERNEST	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,629	KUO ET AL.	
	Examiner	Art Unit	
	Ernest Unelus	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/18/04, 12/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/803,629 has a total of 20 claims pending in the application; there are 3 independent claims and 17 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

3. The applicant's drawings submitted are acceptable for examination purposes.

III. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

4. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statements dated March 18, 2004 and December 19, 2005 are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

IV. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. **Claims 13-20** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In page 32 in the applicant's specification, subject matter such as radio frequency and light wave transmissions are non-statutory embodiments.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claims 1, 9, and 13** recite the limitation "storing data relating to the switch". The "switch" is not clear. The "switch" can be a physical switch or an actual change of context. There is insufficient antecedent basis for this limitation in the claim.

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. **Claims 1-20**, are rejected under 35 U.S.C. 102(b) as being anticipated by

Tojima et al. (US pub. 2002/0026543).

11. As per **claims 1 and 9**, **Tojima** discloses "a method for managing direct memory access resources **(see fig. 1)**, the method comprising: responsive to a change in context for a direct memory access resource **(paragraph 0095 discloses "The priority level decoder 201 decodes the priority level of an inputted DMA transfer request to determine a register where the request is to be stored", as the decoder decode, it's determining the priority level of a request, which is a form of responding to changes in the context)**, storing data relating to the switch in a context switch history **(parameter memory 105 in fig. 1)** containing a number of prior context switches occurring prior to a current context **(paragraph 0099 discloses "Initially, the processor 111 stores parameters required for execution of DMA transfer in the DMA parameter memory 105 through the local bus. The parameters are as follows: read/write information, access unit information such as byte or word, access information indicating consecutive access, rectangle access, ring pointer access, or the like, various kinds of address information such as start address, and the number of transfers". As the paragraph discloses, these parameters about previous context switches are stored prior to a current context. Also disclose, in paragraph 0246, "As described above, according to the eighth embodiment of the invention, since the number of repetition is designated, the processor (DMA transfer request source) does not need to make plural requests of the same DMA transfer, whereby the request issuing process is simplified. This facilitates the hardware design of the processor, and the software design such as programming of the processor. As the result, the load on development is reduced, and the easiness of development is increased**"; and freeing portions of the direct memory access chain of requests using the context switch

history to form freed portions **(paragraph 0097 discloses "The selector 202 selects the resource type information outputted from the priority-level reservation registers 211-213", as the selector selects a request out of any resources (portions), that resource (portion) becomes free once the request that is inside of it leaves)**, wherein the freed portions are reused for requests **(once a request leaves, that space becomes available for a new request to come into it)**.

12. As per **claims 2, 10, and 14, Tojima** discloses "the method of claim 1 **(see rejection to claim 1 above)**, "wherein the portions are direct memory access queues" **(the queues are seen as priority level basis resources C, B, and A).**

13. As per **claims 3, 11, and 15, Tojima** discloses "wherein the freeing step comprises: responsive to processing of requests **(The priority level decoder 201 decodes the priority level of an inputted DMA transfer request to determine a register where the request is to be stored", as the decoder decode, it's determining the priority level of a request, which is a form of responding to processing of request)**, identifying a direct memory access queue for contexts prior to the current context to form an identified direct memory access queue **(paragraph 0095 stated "and resource type information (resource A, B, or C) is stored in each priority-level reservation register. Each priority-level reservation register is provided with a setting register for holding the resource type information. When reservations are made to the respective priority-level reservation registers 211-213, reservation flags 1-3 corresponding to the respective registers 211-213 are set Further")**; and freeing the identified

direct memory access queue **(once a request leaves, that space becomes available for a new request to come into it).**

14. As per **claims 4 and 16, Tojima** discloses, "wherein the context switch history includes a pointer **(reservation pointer register 621)** to a private structure **(the reservation register being a private structure)** for rendering **(which is to present)** the context **(which is the circumstances in which an event occurs) (see paragraph 0182 and fig. 8)**, a pointer **(the pointer for reservation register 610)** to a registration structure for pools of queues **(the queues are seen as priority level basis resources C, B, and A)** linked to the context **(see fig. 8)**, and an identifier for the thread **(automatically, each request discloses the sender's identity; in other word, where the information is coming from, as discloses in paragraph 0099)**

15. As per **claims 5 and 17, Tojima** discloses, "wherein the context switch history is a circular list of a number of context switches" **(according to paragraph 0053 of the applicant's specification, which discloses that circular is to list the request in a chain, such as a "chain of requests", similar, Tojima discloses, in fig. 2, a chain of requests. This chain is made up resources C, B, and A. Requests will be process from priority level 1 to priority level 3 and back around again to level 1.**

16. As per **claims 6 and 18, Tojima** discloses "wherein the change in context occurs when the direct access memory resource is available by a first thread and access to the direct access memory resource is granted to a second thread and wherein the direct access memory resource is

made available to the second thread by adding a buffer of the second thread to an end of a direct memory access chain of requests for the first thread to generate a direct memory access request for the second thread **(Tojima discloses, in paragraph 0097, one request from a first thread or a transfer channel will be process and that available space or ownership to the DMA will be given to the next request from a second thread or transfer channel on line)**.

17. As per **claims 7 and 19, Tojima** discloses, "wherein the direct memory access request is a zero length direct memory access request" **(paragraph 0163 discloses "Thereby, the reservation flags 1, 2, and 3 will be set to "0", "0", and "1", respectively, at the time when the currently executed DMA transfer between the local memory C and the main memory 110 is completed". Each DMA transfer is start on a zero time length).**

18. As per **claims 8, 12, and 20, Tojima** discloses "responsive to encountering an error from a parameter in a request in the direct memory access chain of requests **(paragraph 0032 discloses, "Further, the DMA controller can flexibly cope with various kinds of error processing and application requests, which occur during system operation, whereby the system performance is improved, resulting in a higher-performance system ")**, identifying a queue originating the parameter in the direct memory access chain of requests using the context switch history **(paragraph 0099 discloses "Initially, the processor 111 stores parameters required for execution of DMA transfer in the DMA parameter memory 105 through the local bus. The parameters are as follows: read/write information, access unit information such as byte or word, access information indicating consecutive access, rectangle access, ring pointer access, or the like, various kinds of address information such as start address,**

and the number of transfers". As the paragraph discloses, these parameters about previous context switches are stored prior to a current context". Paragraph 0246 also stated "As described above, according to the eighth embodiment of the invention, since the number of repetition is designated, the processor (DMA transfer request source) does not need to make plural requests of the same DMA transfer, whereby the request issuing process is simplified. This facilitates the hardware design of the processor, and the software design such as programming of the processor. As the result, the load on development is reduced, and the easiness of development is increased "), wherein a bad hardware address is identified using the queue" **(paragraph 0133 discloses "While in this second embodiment the DMA transfer request sources are processors, the sub processor may be implemented by hardware.)**

19. As per **claim 13**, **Tojima** discloses "a computer program **(see paragraphs 0033)** in a computer readable medium for managing direct memory access resources, the computer program product comprising: first instruction, responsive to a change in context for a direct memory access resource **(paragraph 0095 discloses "The priority level decoder 201 decodes the priority level of an inputted DMA transfer request to determine a register where the request is to be stored", as the decoder decode, it's determining the priority level of a request, which is a form of responding to changes in the context)**, storing data relating to the switch in a context switch history **(parameter memory 105 in fig. 1)** containing a number of prior context switches occurring prior to a current context **(paragraph 0099 discloses "Initially, the processor 111 stores parameters required for execution of DMA transfer in the DMA**

parameter memory 105 through the local bus. The parameters are as follows: read/write information, access unit information such as byte or word, access information indicating consecutive access, rectangle access, ring pointer access, or the like, various kinds of address information such as start address, and the number of transfers". As the paragraph discloses, these parameters about previous context switches are stored prior to a current context. Also disclose, in paragraph 0246, "As described above, according to the eighth embodiment of the invention, since the number of repetition is designated, the processor (DMA transfer request source) does not need to make plural requests of the same DMA transfer, whereby the request issuing process is simplified. This facilitates the hardware design of the processor, and the software design such as programming of the processor. As the result, the load on development is reduced, and the easiness of development is increased "); and second instruction for freeing portions of the direct memory access chain of requests using the context switch history to form freed portions **(paragraph 0097 discloses "The selector 202 selects the resource type information outputted from the priority-level reservation registers 211-213", as the selector selects a request out of any resources (portions), that resource (portion) becomes free once the request that is inside of it leaves),** wherein the freed portions are reused for requests **(once a request leaves, that space becomes available for a new request to come into it).**

VI. RELEVANT ART CITED BY THE EXAMINER

20. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

21. The following reference teaches a method for managing a direct memory access resources environment.

U.S. PATENT

US 5,974,480

US 2002/0108003

US 2005/0138235

US 6,954,818

VII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

22. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

23. Per the instant office action, claims 1-20 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

25. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 12, 2006

Ernest Unelus
Examiner
Art Unit 2187

DONALD SPARKS
SUPERVISORY PATENT EXAMINER